This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1- 19. Canceled.

20. (Previously Presented) A photodetector for processing low luminous intensities comprising a monolithically integrated transimpedance amplifier and evaluation electronics, the photodetector having two opposite chip sides, and light (L) being incident from one of the chip sides, the photodetector further comprising

a photocell portion (20) associated with one of the chip sides;

an electronic circuit portion (30) formed on the other of the chip sides, opposite said photocell portion (20);

electric connections between said photocell portion (20) and the electronic circuit portion (30), said electric connections extending in a direction parallel to an axis, said axis being orthogonal as a chip normal with respect to a chip plane, said chip plane being parallel to each of the opposite chip sides;

wherein said electric connections between said photocell portion (20) and said electronic circuit portion (30) are formed by filled trenches doped in specified areas that are extending in a crystalline semiconductor.

21. (Previously Presented) The photodetector of claim 20, wherein said filled trenches comprise conductively doped sidewalls forming electric connections between said photocell portion (20) and said electronic circuit portion (30).

22. (Previously Presented) The photodetector of claim 21, wherein the filled trenches extend entirely through the crystalline semiconductor.

23. (Previously Presented) The photodetector of claim 20, the light being incident from the side associated with the photocell portion (20).

24. (Previously Presented) A photodetector for processing low luminous intensities comprising a monolithically integrated transimpedance amplifier and evaluation electronics, the photodetector having two opposed chip sides, and further comprising

a photocell portion (20) associated with one of the chip sides;

an electronic circuit portion (30) formed on the other of the chip sides, opposite said photo cell portion (20);

electric connections between said photocell portion (20) and the electronic circuit portion (30), said electric connections extending in a direction parallel to an axis, said axis being orthogonal as a chip normal with respect to a chip plane, said chip plane being parallel to each of the chip sides;

wherein filled trenches are provided and filled with a doped polysilicon for establishing said electric connections between said photocell portion (20) and said electronic circuit portion (30) and light (L) being incident from one of the chip sides.

25. (Previously Presented) The photodetector of claim 20, wherein said filled trenches are also used for an electrically non-conductive isolation of different chip areas.

26. (Previously Presented) The photodetector of claim 20, said photodetector being formed by a CMOS or BiCMOS process.

27. (Previously Presented) A method for forming a photodetector according to claim 20 for processing low luminous intensities, said photodetector comprising a monolithically integrated transimpedance amplifier and evaluation electronics (30), the method comprising the steps of:

- using high-ohmic silicon of a first conductivity type in a wafer as an initial material, the wafer having two sides;
- forming an area of inverse conductivity type by counter-doping using on a mask and subsequently annealing a wafer side receiving the evaluation electronics (30);
- performing an epitaxy process and forming a layer having a thickness of substantially 10 to 25 µm, the first conductivity type of the initial material having a doping in a range of 5 to 50 Ohm*cm on one of the wafer sides, as a first wafer side;
- contacting the counter-doped layer, being buried, by locally providing a doping of the epitaxy layer by one of a Sinker diffusion and filled trenches comprising doped areas;
- planarizing at least said filled trenches of the surface of the wafer side including said epitaxy layer;

- performing one of a CMOS and BiCMOS process for forming the integrated electronic circuit (30) on the first wafer side;

- thinning the wafer at the other of the two wafer sides as second side.

28. (Previously Presented) The method of claim 27, for forming the photodetector, wherein after a separating, separated chips are mounted with said one side as detector side on a COL as chip on lead carrier strip, and said mounted chips are electrically connected by bond wires.

29. (Previously Presented) The method of claim 27 for forming the photodetector, wherein after a separating at least one of the separated chips is mounted with the side of the electronic circuit on a printed board or a lead frame or a chip carrier strip;

sealing the mounted chip with a sealing material (61) that is optically transparent in a sensitivity range of said photodetector.

30. (Previously Presented) A photodetector for processing low luminous intensities comprising monolithically integrated transimpedance amplifiers and evaluation electronics as photocell portion and evaluation electronics, formed in a common single crystalline semiconductor material as chip

the photocell portion being buried and an overlying electronic circuit portions being associated with a chip front side of the chip;

electric connections provided as trenches (40, 41) between said buried photocell portion and the electronic circuit portion, said electric connections extending in a direction of a chip normal or parallel with said chip normal;

wherein light to be detected is received from a backside of the chip.

31. (Previously Presented) The monolithic photodetector of claim 30, wherein said chip back side is configured for receiving said light to be detected.

32. (Previously Presented) The monolithic photodetector of claim 30, wherein said electric connections between said photocell portion and said electronic circuit are formed by filled trenches doped in specified areas that are entirely extending within said crystalline semiconductor material.

33. (Previously Presented) The monolithic photodetector of claim 30, wherein said filled trenches extend entirely within said single crystalline semiconductor material and comprise sidewalls (41a, 41b) that are doped along an entire length so as to be conductive along the entire length, and form electric connections between said photocell portion and said electronic circuit portions.

34. (Previously Presented) The monolithic photodetector of claim 30, wherein said filled trenches (41) are filled with doped polysilicon for establishing said electric connections between said photocell and said electronic circuit portions.

35. (Previously Presented) The monolithic photodetector of claim 30, wherein said filled trenches provide for an electrically non-conductive isolation of different chip areas of the chip.

36. (Previously Presented) The monolithic photodetector of claim 30, wherein said photodetector is formed by a CMOS or BiCMOS process.

37. (Currently Amended) A method for forming a photodetector ~~for processing low luminous intensities~~ according to claim 20 for processing low luminous intensities, said photodetector comprising a monolithically integrated transimpedance amplifier and evaluation electronics in a semiconductor wafer, the method having the following manufacturing steps of:

1) using high-ohmic silicon of 100 to 1000 Ohm*cm of a first conductivity type,

2) forming an area of inverse conductivity type by counter-doping based on a mask by ion implantation, and subsequently annealing the wafer front side for carrying the evaluation electronics in a later stage;

3) performing an epitaxy process for forming a layer having a thickness of 10 to 25 µm and the first conductivity type of the initial material having a doping in a range of 5 to 50 Ohm*cm at a wafer front side,

A1) contacting the counter-doped mask defined layer now being buried by filled trenches,

A2) planarizing said filled trenches of the wafer front side,

4) performing one of a standard CMOS and BiCMOS process for forming an integrated electronic circuit on the wafer front side,

5) thinning the semiconductor wafer from a wafer backside,

6) separating the chips, and mounting the separated chips on a printed board or a lead frame or a chip carrier strip, said wafer front side carrying said electronic circuit facing downwardly, and sealing said chip with a sealing material that is optically transparent in a sensitivity range of said photodetector.

38. (Previously Presented) The method of claim 37, wherein a sequence of steps is the sequence of claim 37 as steps 37.1 to 37.6.

39. (Previously Presented) The method of claim 37, wherein the steps 37.A1 and the subsequent step 37.A2 are always performed after step 37.3 or alternatively after step 37.4 or within the process of step 37.4.

40. (Previously Presented) The method of claim 27, comprising the steps of separating and mounting the separated chips and sealing the mounted chips with a sealing material that is optically transparent in a sensitive range of said photodetector.

41. (Previously Presented) Method of claim 27, including a forming of an antireflective coating above said one wafer side.